AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "CROSS-REFERENCE TO RELATED APPLICATIONS" in its entirety and substitute the following section therefor:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/424115, filed on 11/5/02, which is herein incorporated by reference for all intents and purposes.

[0002] This application is related to the following co-pending U.S. Patent ~~Applications~~Application Serial No. 10/682351 (Docket: CNTR.2120), entitled "INTEGRATED CIRCUIT TIMING DEBUG APPARATUS AND METHOD," filed on 10/09/2003. The aforementioned application is now issued as U.S. Patent No. 6903582.~~; which are filed on the same day as this application, and which have a common assignee and common inventors.~~

~~SERIAL NUMBER~~	~~DOCKET NUMBER~~	~~TITLE~~
————	~~CNTR.2120~~	~~MICROPROCESSOR CLOCK VARIATION APPARATUS AND METHOD~~

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0010] An integrated circuit (IC) according to an embodiment of the present invention includes skew-programmable clock buffers, ~~fixed skew logic~~fixed skew logic circuit, an external interface and a skew controller. Each skew-programmable clock buffer receives a distributed clock signal and provides a corresponding local clock signal having a programmed skew. The ~~fixed skew logic~~fixed skew logic circuit enables permanent programming of static skew values and the external interface enables programming of dynamic skew values. The skew controller selects between the static and dynamic skew values and programs the skew-programmable clock buffers based on selected skew values.

[0011] In one embodiment, the skew controller is operative to detect a skew over-ride command upon reset of the IC and to select between the static and dynamic skew values based on the skew over-ride command. The programmable memory may be integrated on the IC or externally coupled via the external interface. The ~~fixed skew logic~~fixed skew logic circuit is implemented as any type of permanent programmable block, such as laser-blown fuses, an EPROM, etc.

[0012] A method of tuning clock skews for an IC according to an embodiment of the present invention includes determining, by the IC upon reset, whether a skew over-ride command is provided, selecting skew values from ~~fixed skew logic~~fixed skew logic circuit integrated on the IC if the skew over-ride command is not provided, selecting skew values from a skew memory if the skew over-ride command is provided, programming at least one programmable delay block integrated on the IC based on selected skew values, and receiving, by each delay block, a distributed clock signal and providing at least one local clock signal having a skew based on a selected skew value.

[0013] The method may include integrating the skew memory as a dynamic memory on the IC and programming the skew memory via an external interface. The method may further include programming a skew over-ride bit on the IC and reading the skew over-ride bit upon reset of the IC. The method may further include holding the IC in reset while programming the skew memory and the skew over-ride bit. The method may further include testing the IC programmed with the dynamic skew values, repeating the programming and testing to determine an optimum set of skew values, and programming the ~~fixed skew logic~~fixed skew logic circuit with the optimum set of skew values.

[0014] A system for fine tuning clock signals of an IC according to an embodiment of the present invention includes a permanent programmable block for permanently programming at least one fixed skew value, ~~programmable logic~~programmable logic circuit for storing at least one dynamic skew value, at least one clock buffer, and a skew controller that selects between the fixed skew value and the dynamic skew value and that programs the clock buffer using the selected skew value. Each clock buffer includes programmable delay logic that delays a clock signal based on a selected skew value.